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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/541,780	04/03/2000	Steve Nishimoto	INLT-0349-US(P8539)	4975

7590 08/22/2002

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EXAMINER
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ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 08/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/541,780	NISHIMOTO, STEVE	
	Examiner	Art Unit	
	Christopher E. Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to because

a) The line CLK is disconnected from the circuit components in Fig. 1.

b) The line crossing and circuit connecting points should be expressed as a dot in Fig. 1 and 9.

c) All related elements in a drawing should be located under one figure number. Therefore, the Fig. 4-8 should be integrated into one figure and located under one figure number.

d) The timing diagram in Fig. 4 through Fig. 8 is incorrect in light of the specification.

e) Substitute "DATA 1" by --DATA IN-- in Fig. 9, based on the specification (page 4, line 12).

f) There is not a reference sign 168 in Fig. 10. It should be in Fig. 10 in light of the specification (page 7, line 23).

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because

1) the reference characters "14" and "14a", "14" and "14b" and "14" and "14c" in Fig. 2 have both been used to designate double pump cells, and

2) the reference characters "100" and "100a", "100" and "100b" and "100" and "100c" in Fig. 12 have both been used to designate double pump cells. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "14" has been used to designate both cell and double pumped bus system. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Note the reference sign 10 on page 1, line 22. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Note the reference sign 40 in Fig. 2. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

6. The drawing in Fig. 12 is objected to because the cell 200 is filtering out the bits from the second set of data, which is caused by the de-asserted EN signal of the cell, in contrary to the specification states the cell 200 is to arrange bits from the two different data sets (i.e., first and second data sets) in a time interleaved fashion (See page 8, lines 22-24). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

7. The application does not have a *brief summary of the invention* in the specification.

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.

(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
(e) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(f) BRIEF SUMMARY OF THE INVENTION.
(g) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(h) DETAILED DESCRIPTION OF THE INVENTION.
(i) CLAIM OR CLAIMS (commencing on a separate sheet).
(j) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(k) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

8. The disclosure is objected to because of the following informalities:

a) On page 3, line 10, substitute "the portion 50" by --the portion 52--.

b) On page 5, line 28, substitute "the bit latch 106" by --the bit latch 102--.

c) On page 6, line 24, substitute "PMOSFET 144" by --PMOSFET 142--.

d) On page 7, line 7, substitute "the bit latch 140" by --the bit latch 104--.

e) On page 7, line 28 and page 8, line 4, substitute "multiplex 160" by --multiplex 106--.

Appropriate correction is required.

Claim Objections

9. Claim 16 is objected to because of the following informalities: The term "form" in the claim makes the examiner confuse to understand the claim based on the specification. The examiner considers it as "from" in light of its parent claim 15. Appropriate correction is required.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

11. Claim 22 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The applicant recites the term "latching the second indications one bit at a time" in the claim 22. However, the claim 22 couldn't be enabled all the time because the term in the claim 22 cannot be justified when it is in the second mode in light of the parent claim 20.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1-9 and 15-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art [hereinafter, AAPA] in view of Tjandrasuwita [USPN 6,049,883].

Referring to claim 1, AAPA discloses an apparatus (cell 12 of double pumped bus system in Fig. 1) comprising: a first circuit (latch 16 and latch 18 of Fig. 1 as combined) to receive indications of first data associated with a first data set (i.e., a signal DATA 1 indicating the bits of the first data set; See page 2, line 9) and second data associated with a second data set (i.e., a signal DATA 2 indicating the bits of the second data set; See page 2, line 10); and a second circuit (multiplexer 20 of Fig. 1) coupled to said first circuit to cause said first circuit to (See Fig. 1): in a first mode (i.e., mode of cell 12 embodiment in Fig. 1), communicate indications of said first data (i.e., furnishing bits of said first data; See page 2, lines 6-7) to an output terminal (wire 26 of Fig. 1) in synchronization (See page 2, lines 21-23) with a first phase of a clock signal (i.e., negative edge of CLK signal; See page 2, lines 14-15) and communicate

indications of said second data (i.e., furnishing bits of said second data; See page 2, lines 7-8) to said output terminal (wire 26 of Fig. 1) in synchronization (See page 2, lines 21-23) with a second phase of said clock signal (i.e., positive edge of CLK signal; See page 2, lines 17-19). AAPA does not disclose a clock gating apparatus for a mode control, wherein said first circuit to prevent communication of said second data during said second phase of clock signal. Tjandrasuwita discloses a clock gating apparatus, wherein a circuit (latch circuit 502 of Fig. 5) to prevent communication (i.e., disable EN2 501 of the AND gate input in Fig. 5) of a data (i.e., serial data stream; See col. 6, line 37) during a phase of clock signal (e.g., positive edge of Clock 406 of Fig. 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said clock gating apparatus, as disclosed by Tjandrasuwita, in said apparatus (i.e., double pumped bus system), as disclosed by AAPA, so that said apparatus could control (i.e., allowing or preventing) said communication of said second data during said second phase. AAPA, as modified by Tjandrasuwita, teaches a second mode, wherein said first circuit (latches in Fig. 1 as combined of AAPA) communicates said indications of said first data (i.e., furnishing bits of said first data; See page 2, lines 6-7 of AAPA) to said output terminal (wire 26 of Fig. 1 of AAPA) in synchronization (See page 2, lines 21-23 of AAPA) with said first phase (i.e., negative edge of CLK signal; See page 2, lines 14-15 of AAPA) and prevents communication (i.e., disable EN2 501 of the AND gate input in Fig. 5 of Tjandrasuwita) of said second data (i.e., serial data stream; See col. 6, line 37 of Tjandrasuwita) during said second phase (e.g., positive edge of Clock 406 of Fig. 5 from Tjandrasuwita).

Referring to claim 2, AAPA discloses said first circuit comprises: a first latch (bit latch 16 in cell 12 of Fig. 1) to store at least one bit at a time of said first data; and a second latch (bit latch 18 in cell 12 of Fig. 1), at least in said first mode (See the claim 1 rejection in terms of the clock gating), store at least one bit at a time of said second data (See page 2, lines 14-20).

Referring to claim 3, AAPA discloses said first latch (i.e., bit latch 16 in cell 12 of Fig. 1) transfers said at least one bit of said first data in response to a predefined edge (i.e., negative edge) of said clock signal (See page 2, lines 11-20).

Referring to claim 4, AAPA discloses said second latch (i.e., bit latch 18 of cell 12 of Fig. 1) transfers said at least one bit of said second data in response to a predefined edge (i.e., positive edge) of said clock signal (See page 2, lines 11-20) in said first mode (See the claim 1 rejection in terms of the first mode).

Referring to claim 5, AAPA , as modified by Tjandrasuwita, discloses logic (i.e., clock gating in Fig. 5 of Tjandrasuwita) to selectively (i.e., whether EN2 503 is set to enable or disable in Fig. 5; Tjandrasuwita) provide said clock signal to said second latch based on whether said apparatus is in said first (i.e., in case of EN2 is enabled; Tjandrasuwita) or second mode (i.e., in case of EN2 is disabled; Tjandrasuwita).

Referring to claim 6, AAPA , as modified by Tjandrasuwita, discloses said logic does not provide said clock signal (i.e., when EN2 is disabled; Refer to the clock gating logic in Fig. 5, which is consisted of AND gate 503, EN2 input and Clock input 406; Tjandrasuwita) to said second latch in said second mode.

Referring to claim 7, AAPA , as modified by Tjandrasuwita, discloses said logic comprises: an AND gate (gate 503 of Fig 5; Tjandrasuwita) including a first input terminal (EN2 in Fig. 5 of Tjandrasuwita) to receive a mode select signal (i.e., EN2 is enabled when said mode is set to said first mode, and EN2 is disabled when said mode is set to said second mode), a second input terminal (Clock signal 406 of Fig. 5 from Tjandrasuwita) to receive said clock signal and an output terminal (i.e., output of said AND gate 503 of Fig 5. from Tjandrasuwita) coupled to a clock input terminal (CLK of latch 502 of Fig. 5 from Tjandrasuwita) of said second latch.

Referring to claim 8, AAPA discloses a multiplexer 20 (Fig. 1) including an output terminal (i.e., output of said multiplexer 20 in Fig. 1) that is coupled to said output terminal (wire 26 of Fig. 1) of said apparatus (cell 12 of double pumped bus system in Fig. 1), said multiplexer alternatively selecting said first and second latch in response to said first and second phases of said clock signal (See page 1, lines 24-28 and page 2, lines 21-23).

Referring to claim 9, AAPA discloses said apparatus comprises a double pumped bus circuit (See Fig. 1 and 2).

Referring to claim 15, AAPA discloses a system (double pumped bus system in Fig. 2) comprising: double pumped bus circuits serially coupled together to form a chain to communicate data from at least two different sets of data (See page 2, lines 1-3). AAPA does not disclose at least one of said bus circuits being capable of being disabled to prevent bits from at least one of said sets of data from communicated through said at least of said bus circuits. Tjandrasuwita discloses a clock gating apparatus, wherein a circuit (latch circuit 502 of Fig. 5) to prevent communication (i.e., disable EN2 501 of the AND gate input in Fig. 5) of a data (i.e., serial data stream; See col. 6, line 37) during a phase of clock signal (e.g., positive edge of Clock 406 of Fig. 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said clock gating apparatus, as disclosed by Tjandrasuwita, in said apparatus (i.e., double pumped bus system), as disclosed by AAPA, so that said apparatus could control (i.e., allowing or preventing) said communication of said second data during said second phase. AAPA, as modified by Tjandrasuwita, teaches at least one of said bus circuits being capable of being disabled (i.e., EN2 501 of Fig. 5 is disabled; Tjandrasuwita) to prevent bits from at least one of said sets of data (i.e., DATA 1 or DATA 2 in Fig. 1 of AAPA) from communicated through said at least of said bus circuits (i.e., disable EN2 501 of the AND gate input in Fig. 5 of Tjandrasuwita).

Referring to claim 17, AAPA discloses each double pumped circuit latches bits (i.e., latches bits using bit latches 16 and 18 in cell 12 of Fig. 1) from one of said sets of data (i.e., DATA 1 or DATA 2 in

Fig. 1) in response to first edges (i.e., positive or negative edges) of a clock signal (See page 2, lines 11-13) and furnishes indications of said bits in response to second edges (i.e., negative or positive edges) of said clock signal (See page 2, lines 14-20), said first edges being different from said second edges (i.e., a first circuit latches a bit of a first data set at a first edge of a clock signal and a system furnishes a latched bit of a second data set at said first edge of said clock signal, then a second circuit latches a bit of said second data set at a second edge of said clock signal and said system furnishes said latched bit of said first data set at said second edge of said clock signal; See the prior art in the background of AAPA).

Referring to claims 18-19, AAPA teaches said first edges in said system comprises positive edges or negative edges of said clock signal under the condition of mutually exclusive application (See page 2, lines 6-20).

Referring to claim 20, the method steps of claim 20 are inherently performed by the apparatus of claim 1, and therefore the rejection of claim 1 applies to claim 20.

Referring to claim 21, the method steps of claim 21 are inherently performed by the apparatus of claim 2, and therefore the rejection of claim 2 applies to claim 21.

Referring to claim 22, the method steps of claim 22 are inherently performed by the apparatus of claim 2, at least in said first mode, and therefore the rejection of claim 2 applies to claim 22. In said second mode, this claim is rejected under 35 U.S.C. 112, first paragraph, Enablement problem.

Referring to claim 23, AAPA discloses said method of claim 20, wherein said communicating during said first mode comprise: communicating bits of said first data (i.e., DATA 1 in Fig. 1) in response to first predefined edges (i.e., positive edges) of said clock signal; and communicating a bits of said second data (i.e., DATA 2 in Fig. 1) in response to other predefined edges (i.e., negative edges) being different from said first predefined clock edges (i.e., a first circuit latches a bit of a first data set at a first edge of a clock signal and a system furnishes a latched bit of a second data set at said first edge of said clock signal, then a second circuit latches a bit of said second data set at a second edge of said clock

signal and said system furnishes said latched bit of said first data set at said second edge of said clock signal; See the prior art in the background of AAPA).

14. Claims 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tjandrasuwita [USPN 6,049,883] in view of Applicant Admitted Prior Art [hereinafter, AAPA].

Referring to claim 10, Tjandrasuwita discloses a computer system (computer system 100 of Fig. 3) comprising: a system memory (RAM 304 of Fig. 3); a processor (integrated processor circuit 301 of Fig. 3) coupled to system memory (Fig. 3); and a clock gating apparatus, wherein a circuit (latch circuit 502 of Fig. 5) to prevent communication (i.e., disable EN2 501 of the AND gate input in Fig. 5) of a data (i.e., serial data stream; See col. 6, line 37) during a phase of clock signal (e.g., positive edge of Clock 406 of Fig. 5). Tjandrasuwita does not disclose said processor including: a wire; a first circuit; and a second circuit. AAPA discloses a processor (an apparatus; i.e., cell 12 of double pumped bus system in Fig. 1) including: a wire (wire 26 of Fig. 1); a first circuit (latch 16 and latch 18 of Fig. 1 as combined) to receive indications of first data associated with a first data set (i.e., a signal DATA 1 indicating the bits of the first data set; See page 2, line 9) and second data associated with a second data set (i.e., a signal DATA 2 indicating the bits of the second data set; See page 2, line 10); and a second circuit (multiplexer 20 of Fig. 1) coupled to said first circuit to cause said first circuit to (See Fig. 1): in a first mode (i.e., mode of cell 12 embodiment in Fig. 1), communicate indications of said first data (i.e., furnishing bits of said first data; See page 2, lines 6-7) to said wire (wire 26 of Fig. 1) in synchronization (See page 2, lines 21-23) with a first phase of a clock signal (i.e., negative edge of CLK signal; See page 2, lines 14-15) and communicate indications of said second data (i.e., furnishing bits of said second data; See page 2, lines 7-8) to said wire (wire 26 of Fig. 1) in synchronization (See page 2, lines 21-23) with a second phase of said clock signal (i.e., positive edge of CLK signal; See page 2, lines 17-19). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said apparatus, as disclosed by AAPA, in said computer system, as disclosed by Tjandrasuwita, for the

advantage of reducing the number of wires on said processor of said computer system, which are used to communicate different sets of data (See page 1, lines 9-10). Tjandrasuwita, as modified by AAPA, discloses a second mode, wherein said first circuit (latches in Fig. 1 as combined of AAPA) communicates said indications of said first data (i.e., furnishing bits of said first data; See page 2, lines 6-7 of AAPA) to said output terminal (wire 26 of Fig. 1 of AAPA) in synchronization (See page 2, lines 21-23 of AAPA) with said first phase (i.e., negative edge of CLK signal; See page 2, lines 14-15 of AAPA) and prevents communication (i.e., disable EN2 501 of the AND gate input in Fig. 5 of Tjandrasuwita) of said second data (i.e., serial data stream; See col. 6, line 37 of Tjandrasuwita) during said second phase (e.g., positive edge of Clock 406 of Fig. 5 from Tjandrasuwita).

Referring to claim 11, Tjandrasuwita , as modified by AAPA, discloses said first circuit comprises: a first latch (bit latch 16 in cell 12 of Fig. 1; AAPA) to store at least one bit at a time of said first data; and a second latch (bit latch 18 in cell 12 of Fig. 1; AAPA), at least in said first mode (See the claim 10 rejection in terms of the clock gating), store at least one bit at a time of said second data (See page 2, lines 14-20; AAPA).

Referring to claim 12, Tjandrasuwita , as modified by AAPA, discloses said first latch (i.e., bit latch 16 in cell 12 of Fig. 1; AAPA) transfers said at least one bit of said first data in response to a predefined edge (i.e., negative edge; AAPA) of said clock signal (See page 2, lines 11-20; AAPA).

Referring to claim 13, Tjandrasuwita , as modified by AAPA, discloses said second latch (i.e., bit latch 18 of cell 12 of Fig. 1; AAPA) transfers said at least one bit of said second data in response to a predefined edge (i.e., positive edge; AAPA) of said clock signal (See page 2, lines 11-20; AAPA) in said first mode (See the claim 10 rejection in terms of the first mode).

Referring to claim 14, Tjandrasuwita discloses logic (i.e., clock gating in Fig. 5) to selectively (i.e., whether EN2 503 is set to enable or disable in Fig. 5) provide said clock signal to said second latch

based on whether said apparatus is in said first (i.e., in case of EN2 is enabled) or second mode (i.e., in case of EN2 is disabled).

15. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art [hereinafter, AAPA] in view of Tjandrasuwita [USPN 6,049,883] as applied to claim 15 above, and further in view of Sproch et al. [USPN 6,247,134 B1].

Referring to claim 16, AAPA, as modified by Tjandrasuwita, discloses at least one of said double pumped circuits in said system are disabled (i.e., EN2 501 of Fig. 5 is disabled; Tjandrasuwita) to prevent said bits from at least one of said sets of data (i.e., serial data stream; See col. 6, line 37 of Tjandrasuwita) from being communicated through said at least one of said bus circuits (i.e., disable EN2 501 of the AND gate input in Fig. 5 of Tjandrasuwita). AAPA, as modified by Tjandrasuwita, does not teach alternate double pumped circuits in said system are disabled. Sproch et al. disclose a method and system for pipe stage gating, wherein a stall condition "C" determination circuit 210 (Fig. 8) and a stall signal propagation and clock gating circuit 230 (Fig. 3; i.e., D-latches and AND gates as combined in Fig. 8) alternately disable double pumped circuits (register latches 221,222,223,225 in Fig. 8) when the input operand bit streams are 110011001100... on DATA 1(bus 242a of Fig. 8) and 001100110011... on DATA 2 (bus 242b of Fig. 8). Refer to col. 12, lines 48-51 for the alternate disabling condition of the clock gates 351,352,353 and 355 in Fig. 8. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said apparatus for alternately disabling said register latches, as disclosed by Sproch et al., in said embodiment of alternately disabling double pumped circuits, as disclosed by AAPA in view of Tjandrasuwita, for the advantage of saving power in said double pumped bus when said bus does not care about said input data, e.g., its results are inconsequential because of equality (See col. 3, line 64 through col. 4, line 3 and col. 12, lines 48-53).

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Heinen et al [USPN 5,994,931] disclose method and circuit configuration for controlling operating states of a second device by means of a first device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter S. Wong can be reached on 703-305-3477. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-3718 for regular communications and 703-746-9248 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Christopher E. Lee
Examiner
Art Unit 2181

cel/ CEL
August 19, 2002

PETER WONG
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100